Instruction Manual

Tektronix

TMS 102
80186 & 80188 Microprocessor Support

070-9805-01

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 102 80186/80188 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 102 80186/80188 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with 80186. This is the name of the microprocessor in field selections and file names you must use to operate the 80186/80188 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or 96-channel module.
- 80186 refers to all supported variations of the 80186/80188 microprocessor unless otherwise noted.
- 80186/188 refers to both the 80186 and 80188 microprocessors unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2440) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- A description of the TMS 102 microprocessor support
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to connect to the system under test (SUT)

Support Description

The TMS 102 microprocessor support disassembles data from systems that are based on the Intel 80186/80188 microprocessor. This support also disassembles 8087 floating point coprocessor instructions. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 102 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 102 support can acquire and disassemble data.

Table 1–1: Product support

Microprocessor	Package	Number of pins
80186	PGA, PLCC	68
80188	PGA, PLCC	68

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *80186/80188 Microprocessor User's Manual*, Intel.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 80186/80188 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire clock and channel data from signals in your 80186/80188-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 80186/80188 support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the 80186/80188 microprocessor at speeds of up to 20 MHz[1].

[1] **Specification at time of printing. Contact your logic analyzer sales representative for current information on the fastest devices supported.**

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin 1 indicator on the probe adapter board with the pin 1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–1.

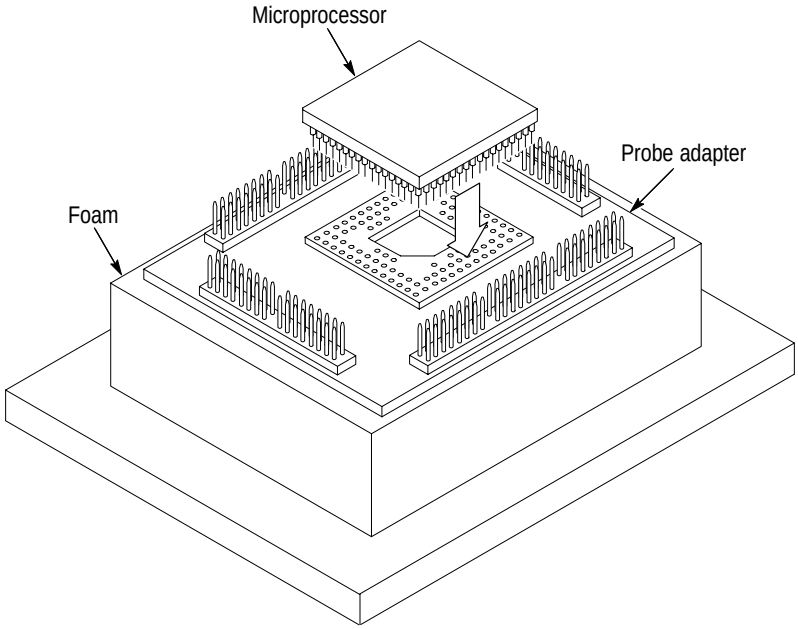


Figure 1–1: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

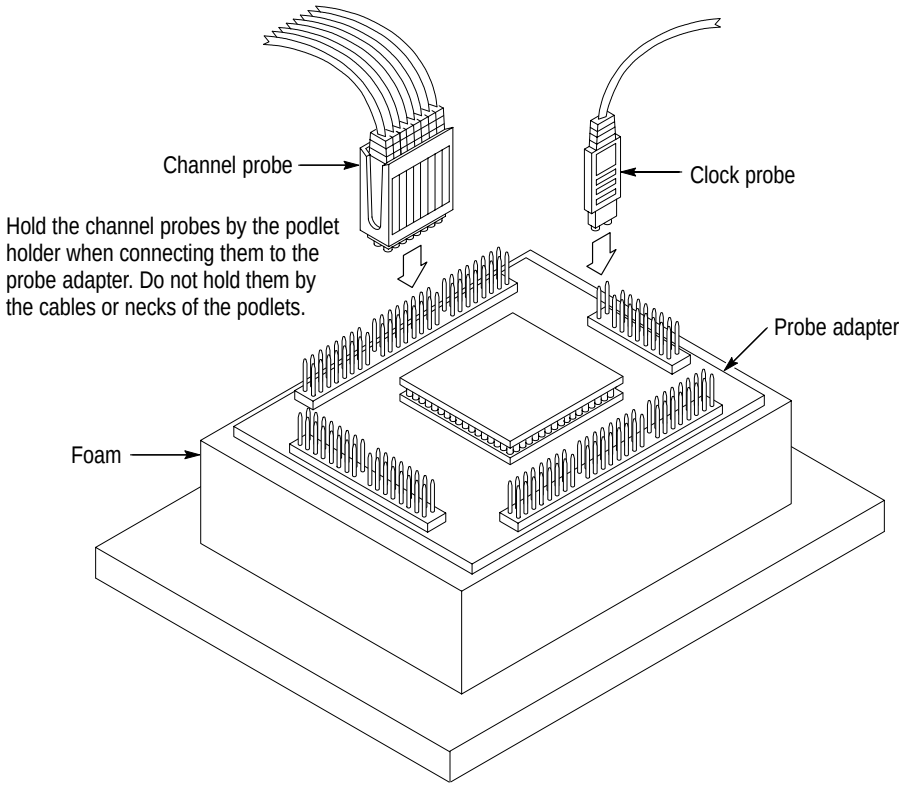


Figure 1–2: Connecting probes to a PGA probe adapter

8. Line up the pin 1 indicator on the probe adapter board with the pin 1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

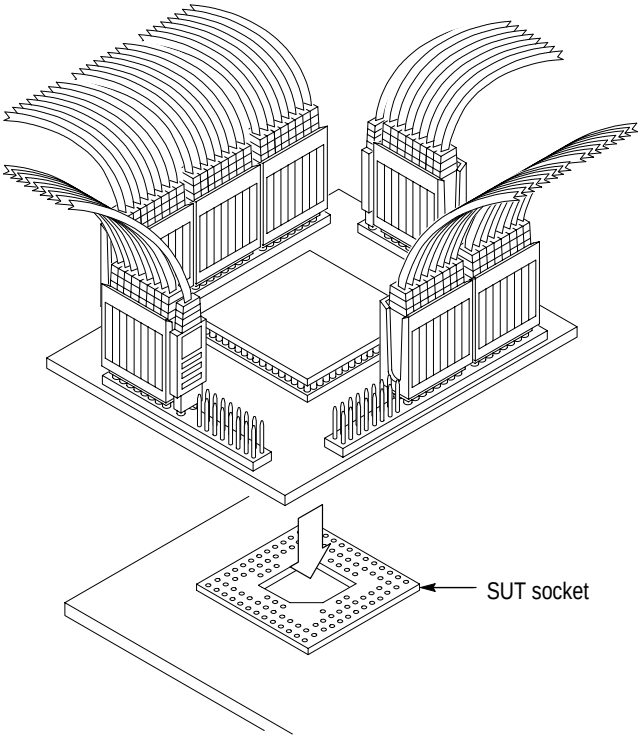


Figure 1–3: Placing a PGA probe adapter onto the SUT

PLCC Probe Adapter

To connect the logic analyzer to a SUT using a PLCC probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–4. This prevents the circuit board from flexing.
4. Remove the microprocessor from your SUT.

5. Line up the pin 1 indicator on the microprocessor with pin 1 of the PLCC socket on the probe adapter.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage all electrical components once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–4.

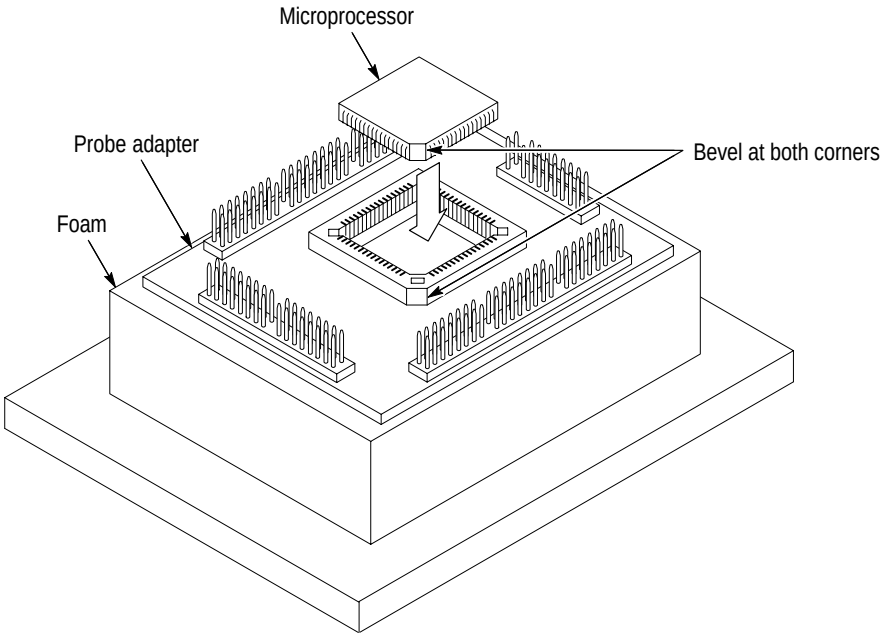


Figure 1–4: Placing a microprocessor into a PLCC probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–5. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

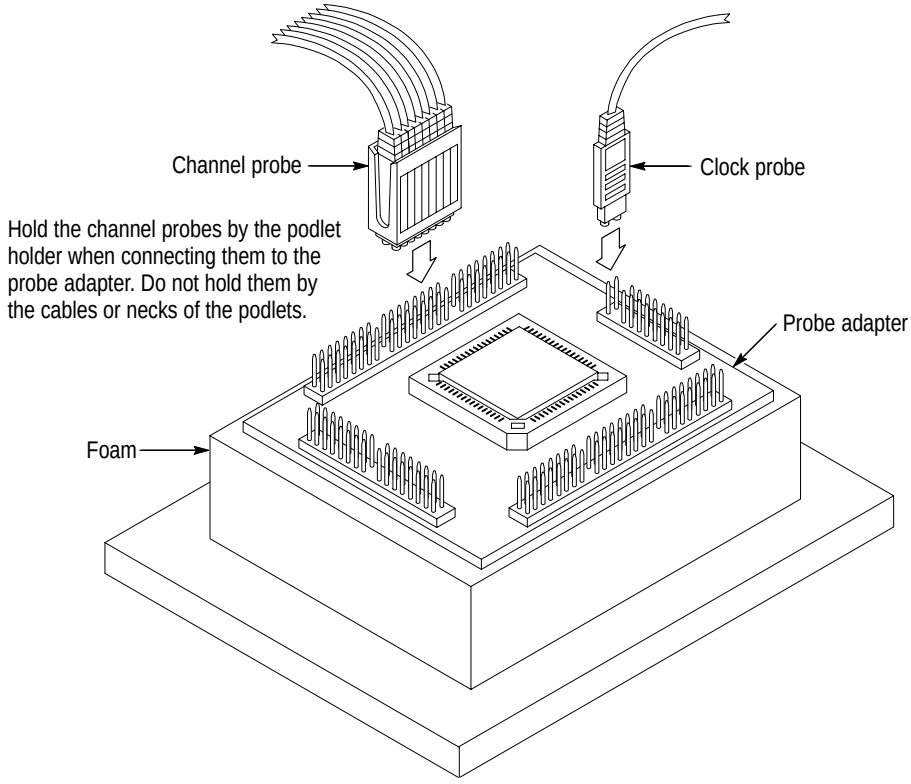


Figure 1–5: Connecting probes to a PLCC probe adapter

8. Place the probe adapter onto the SUT as shown in Figure 1–6.

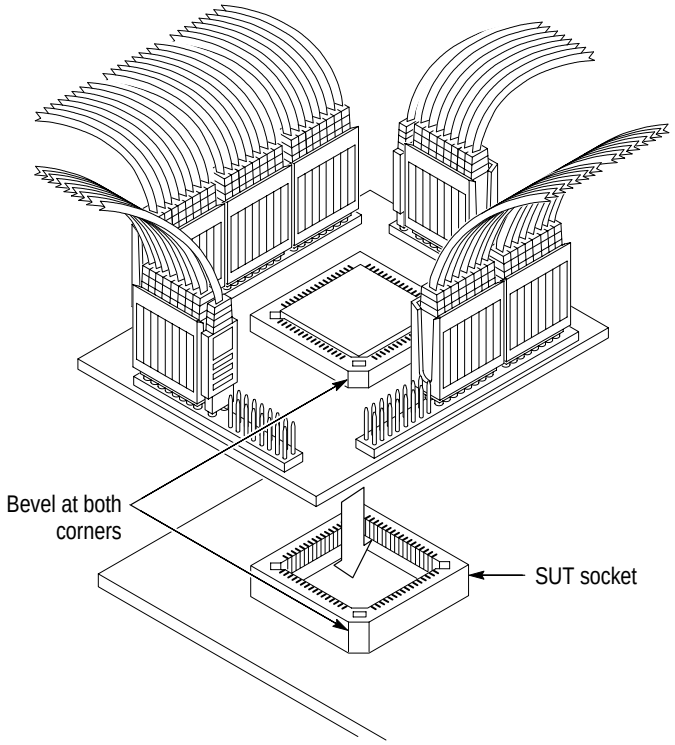


Figure 1–6: Placing a PLCC probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 80186/80188 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. Use Table 1–2 to connect the channel probes to 80186/80188 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–2: 80186/80188 signal connections for channel probes

Section:channel	80186/80188 signal	Section:channel	80186/80188 signal
A3:7	UCS~*	D3:7	CLKOUT_B*
A3:6	LCS~*	D3:6	PCS6~*
A3:5	TMR1OUT*	D3:5	PCS5~*
A3:4	TMR0OUT*	D3:4	PCS4~*
A3:3	TMR1IN*	D3:3	PCS3~*
A3:2	TMR0IN*	D3:2	PCS2~*
A3:1	DRQ1*	D3:1	PCS1~*
A3:0	DRQ0*	D3:0	PCS0~*
A2:7	DT_R~*	D2:7	Not connected
A2:6	DEN~*	D2:6	Not connected
A2:5	HOLD*	D2:5	Not connected
A2:4	BHE~	D2:4	S7*
A2:3	A19/S6	D2:3	S6
A2:2	A18/S5	D2:2	S5*
A2:1	A17/S4	D2:1	S4*
A2:0	A16/S3	D2:0	S3*
A1:7	AD15	D1:7	Not connected
A1:6	AD14	D1:6	Not connected
A1:5	AD13	D1:5	Not connected
A1:4	AD12	D1:4	Not connected
A1:3	AD11	D1:3	Not connected
A1:2	AD10	D1:2	Not connected
A1:1	AD9	D1:1	Not connected
A1:0	AD8	D1:0	Not connected
A0:7	AD7	D0:7	Not connected
A0:6	AD6	D0:6	Not connected

Table 1–2: 80186/80188 signal connections for channel probes (cont.)

Section:channel	80186/80188 signal	Section:channel	80186/80188 signal
A0:5	AD5	D0:5	Not connected
A0:4	AD4	D0:4	Not connected
A0:3	AD3	D0:3	Not connected
A0:2	AD2	D0:2	Not connected
A0:1	AD1	D0:1	Not connected
A0:0	AD0	D0:0	Not connected
C3:7	INT3*	C2:7	TEST~*
C3:6	INT2*	C2:6	NMI*
C3:5	INT1*	C2:5	LOCK~
C3:4	INT0*	C2:4	S2~
C3:3	MCS3~*	C2:3	S1~
C3:2	MCS2~*	C2:2	S0~
C3:1	MCS1~*	C2:1	HLDA
C3:0	MCS0~*	C2:0	RESET
C1:7	Not connected	C0:7	Not connected
C1:6	Not connected	C0:6	Not connected
C1:5	Not connected	C0:5	Not connected
C1:4	Not connected	C0:4	SRDY*
C1:3	Not connected	C0:3	ARDY*
C1:2	Not connected	C0:2	RD~*
C1:1	Not connected	C0:1	WR~*
C1:0	Not connected	C0:0	ALE~*

*** Signal not required for disassembly.**

Table 1–3 shows the clock probes and the 80186/80188 signal to which they must connect for disassembly to be correct.

Table 1–3: 80186/80188 signal connections for clock probes

Section:channel	80186/80188 signal
CK:3	CLKOUT
CK:2	STATUS
CK:1	Not connected
CK:0	Not connected

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 80186/80188 microprocessor in your SUT and attach the clip to the microprocessor.

6. Use the channel assignment tables in the *Specifications* chapter to connect channel and clock probes to your test clip.

7. Use the channel assignment tables in the *Specifications* chapter to connect channel and clock probes to the module probe cables.

8. Connect at least one ground podlet (lead) from each channel probe and the ground from each clock probe to ground pins on your test clip.

9. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the microprocessor in your SUT and attach it to the microprocessor.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 102 80186/80188 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The disassembler software automatically defines channel groups for the support. The channel groups for the 80186/80188 support are Address, Data, Control, Intr, Timers, Chip_Sel, Async, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–5.

Clocking Options

The TMS 102 support offers a microprocessor-specific clocking mode for the 80186/80188 microprocessor. This clocking mode is the default selection whenever you load the 80186 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 102 support is: DMA Cycles.

DMA Cycles

A DMA cycle is defined as the cycle in which the 80186/80188 microprocessor gives up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 102 support supplies two symbol table files. The 80186_Ctrl and 80188_Ctrl files replace specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the files 80186_Ctrl and 80188_Ctrl Control channel group symbol tables.

Table 2–1: Control group symbol table definitions

Symbol	Control group value LOCK~ S6 RESET HLDA S2~ S1~ S0~ BHE~	Meaning
RESET	X X 1 X X X X X	RESET signal asserted
DMA_RDINT	X 1 X 0 X 0 X X	An internal DMA read
DMA_WRINT	X 1 X 0 X 1 X X	An internal DMA write
DMA_INT	X 1 X 0 X X X X	An internal DMA
DMA_RDEXT	X X X 1 X 0 X X	An external DMA read
DMA_WREXT	X X X 1 X 1 X X	An external DMA write
DMA_EXT	X X X 1 X X X X	An external DMA
MEM_READ	1 0 X 0 1 0 1 X	Data read cycle (nonopcode fetch)
MEM_WRITE	1 0 X 0 1 1 0 X	Any memory write
I/O_READ	1 0 X 0 0 0 1 X	Read from I/O space
I/O_WRITE	1 0 X 0 0 1 0 X	Write to I/O space
FETCH	X 0 X 0 1 0 0 X	Code read (opcode fetch)
HALT	X 0 X 0 0 1 1 X	Processor halted
INT_ACK	X 0 X 0 0 0 0 X	Responding to an interrupt
LKD_M_RD	0 0 X 0 1 0 1 X	Locked memory read cycle (nonop-code fetch)
LKD_M_WR	0 0 X 0 1 1 0 X	Locked memory write cycle
LKD_IO_RD	0 0 X 0 0 0 1 X	Locked read from I/O space
LKD_IO_WR	0 0 X 0 0 1 0 X	Locked write to I/O space
READ	X 0 X 0 X 0 1 X	Any memory or I/O read cycle except an Opcode Fetch or Int Ack cycle

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value LOCK~ S6 RESET HLDA S2~ S1~ S0~ BHE~	Meaning
WRITE	X 0 X 0 X 1 0 X	Any memory or I/O write
LOCKED	0 X X X X X X X	Inseparable back-to-back cycles

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 80186/80188 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page for the 102/136-channel module, or in the Disassembly Format Definition overlay for the 96-channel module must be set correctly for your acquired data to be disassembled correctly.* *Refer to* Changing How Data is Displayed *on page 2–8.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
m or >>	The instruction was manually marked
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte.
#	Indicates an immediate value
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(RESET)	The RESET signal is asserted
(DMA RDINT)	An internal direct memory access read cycle
(DMA WRINT)	An internal direct memory access write cycle
(DMA RDEXT)	An external direct memory access read cycle
(DMA WREXT)	An external direct memory access write cycle
(HALT)	The processor is halted
(INT ACK)	An interrupt acknowledge cycle
(I/O READ)	A read from I/O space
(I/O WRITE)	A write to I/O space
(MEM READ)	A read from memory that is not an opcode fetch
(MEM WRITE)	Any write to memory
(LOCKED MEM READ)	A locked read from memory that is not an opcode fetch
(LOCKED MEM WRITE)	A locked write to memeory
(LOCKED I/O READ)	A locked read from I/O space
(LOCKED I/O WRITE)	A locked write to I/O space
(FLUSH)	A fetch cycle computed by the disassembler to be an opcode flush
(EXTENSION)	A fetch cycle computed by the disassembler to be an opcode extension

Table 2–3: Cycle type definitions (Cont.)

Cycle type	Definition
(REFRESH)	A memory refresh cycle, computed by the disassembler
(UNKNOWN)	The combination of bits in the Control channel group is either unexpected or unrecoginzed.

Figure 2–1 shows an example of the Hardware display.

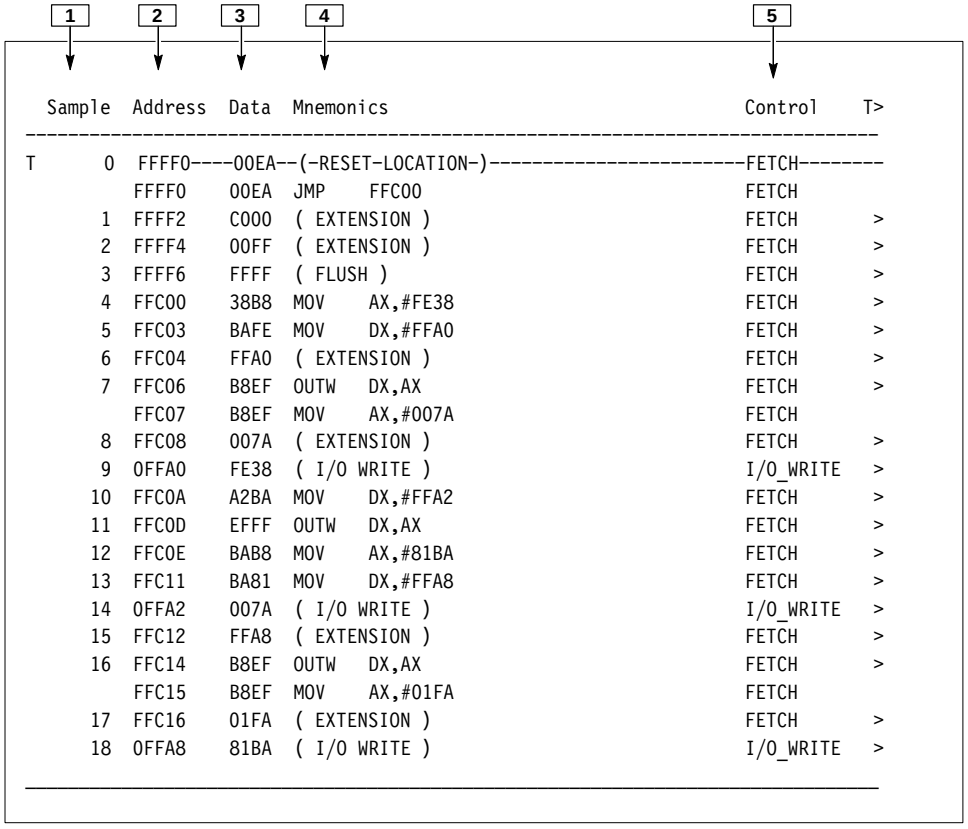


Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 80186/80188 Address bus.

3 **Data Group.** Lists data from channels connected to the 80186/80188 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to the 80186/80188 control bus.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the 80186/80188 microprocessor are as follows:

BOUND	JE	JNO
CALL	JL	JNS
DIV	JLE	JO
IDIV	JMP	JP
INTO	JNB	JS
INTX	JNBE	LOOP
IRET	JNE	LOOPNZ
JB	JNL	LOOPZ
JCXZ	JNLE	RET

Subroutine Display Format

The Subroutine display format shows the first fetch of subroutine calls and return instructions. Instructions that generate a subroutine call or a return in the 80186/80188 microprocessor are as follows:

BOUND	IDIV	IRET
DIV	INTO	RET
CALL	INTX	

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 80186/80188 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no new fields for this support product. Refer to the information on basic operations for discriptions of common fields.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)

Table 2–4 shows the selections for the 80186 microprocessor.

Table 2–4: 80186 prefetch cycles

Program fetch cycle	Description
Opcode	The one-byte cycle will be disassembled as the beginning of an instruction.
Extension	The one-byte cycle is treated as an extension of the previous instruction.
Flush	The one-byte cycle is not disassembled.
Any opcode	The low byte of the cycle will be disassembled as the beginning of an instruction. The high byte is not marked.
Opcode extension	The low byte of the cycle is treated as an instruction extension. The high byte is not marked.
Opcode flush	The low byte of the cycle is not disassembled and the high byte of the cycle is not marked.
Extension-extension	The low byte and the high byte are treated as extensions of the previous instruction.
Flush-flush	The cycle is not disassembled.
Undo marks on this cycle	Marks are removed from the cycle and the disassembly reverts to the premark state.

Table 2–5 shows the selections for the 80188 microprocessor.

Table 2–5: 80188 prefetch cycles

Program fetch cycle	Description
Opcode	The cycle will be disassembled as the beginning of an instruction.
Extension	The cycle is treated as an extension of the previous instruction.
Flush	The cycle is not disassembled.
Undo marks on this cycle	Marks are removed from the cycle and the disassembly reverts to the premark state.

Information on basic operations contains more details on marking cycles.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 80186/80188 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 80186/80188 signals
- List of other accessible microprocessor signals and extra acquisition channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 80186/80188 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The PGA probe adapter accommodates the Intel 80186/80188 microprocessor in a 68-pin PGA package. The PLCC probe adapter accommodates the Intel 80186/80188 microprocessor in a 68-pin PLCC package.

Configuration

The probe adatper does not require any configuration.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) 210 mA I typ (measured) 160 mA	
SUT clock		
Clock rate	Min. DC Max. 20MHz	
Minimum setup time required		
Address, Data	5 ns	
HLDA	6.5 ns	
Relative to CLK rising edge: S0~-S2~ inactive to active	4.5 ns	
Relative to CLK falling edge: S0~-S2~ active to inactive	10 ns	
All Other Signals	5 ns	
Minimum hold time required		
All Signals	0 ns	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
CLKOUT	18 pf + 1 podlet	1, 20R6-5 + 1 podlet
S0*, S1*, S2*	13 pf + 1 podlet	1, 20R6-5 + 1 podlet

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)

Table 3–2: Environmental specification* (cont.)

Characteristic	Description
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed 80186/80188 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
FCC Compliance	Emissions comply with FCC Code of Federal Regulations 47, Part 15, Subpart B, Class A Limits
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

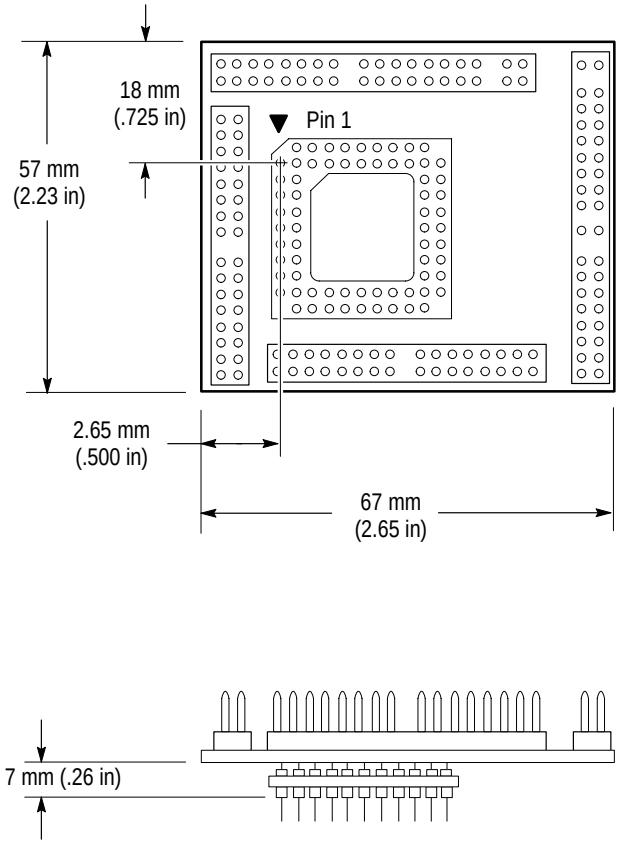


Figure 3–1: Minimum Clearance of the PGA Probe Adapter

Figure 3–2 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

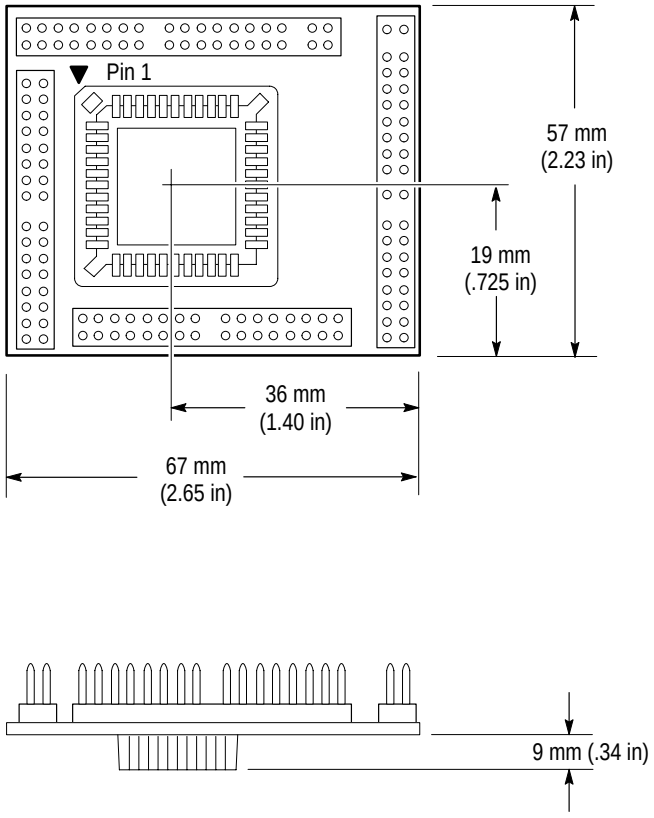


Figure 3–2: Minimum Clearance of the PLCC Probe Adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–12 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	80186/80188 signal name
19	A2:3	A19/S6
18	A2:2	A18/S5
17	A2:1	A17/S4
16	A2:0	A16/S3
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section:channel	80186/80188 signal name
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–6 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–6: Control group channel assignments

Bit order	Section:channel	80186/80188 signal name
7	C2:5	LOCK~
6	D2:3	S6
5	C2:0	RESET
4	C2:1	HLDA
3	C2:4	S2~

Table 3–6: Control group channel assignments (cont.)

Bit order	Section:channel	80186/80188 signal name
2	C2:3	S1~
1	C2:2	S0~
0	A2:4	BHE~

Table 3–7 shows the section and channel assignments for the Interrupt group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: Interrupt group channel assignments

Bit order	Section:channel	80186/80188 signal name
4	C2:6	NMI*
3	C3:7	INT3*
2	C3:6	INT2*
1	C3:5	INT1*
0	C3:4	INT0*

*** Signal not required for disassembly.**

Table 3–8 shows the section and channel assignments for the Timer group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: Timer group channel assignments

Bit order	Section:channel	80186/80188 signal name
3	A3:5	TMR1OUT*
2	A3:4	TMR0OUT*
1	A3:3	TMR1IN*
0	A3:2	TMR0IN*

*** Signal not required for disassembly.**

Table 3–9 shows the section and channel assignments for the Chip_Select group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Chip_Select group channel assignments

Bit order	Section:channel	80186/80188 signal name
12	A3:7	UCS~*
11	A3:6	LCS~*
10	C3:3	MCS3~*
9	C3:2	MCS2~*
8	C3:1	MCS1~*
7	C3:0	MCS0~*
6	D3:6	PCS6~*
5	D3:5	PCS5~*
4	D3:4	PCS4~*
3	D3:3	PCS3~*
2	D3:2	PCS2~*
1	D3:1	PCS1~*
0	D3:0	PCS0~*

*** Signal not required for disassembly.**

Table 3–10 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: Misc group channel assignments

Bit order	Section:channel	80186/80188 signal name
10	D3:7	CLKOUT_B*
9	C2:7	TEST~*
8	A3:1	DRQ1*
7	A3:0	DRQ0*
6	D2:4	S7*
5	D2:2	S5*
4	D2:1	S4*

Table 3–10: Misc group channel assignments (cont.)

Bit order	Section:channel	80186/80188 signal name
3	D2:0	S3*
2	A2:7	DT_R~*
1	A2:6	DEN~*
0	A2:5	HOLD*

*** Signal not required for disassembly.**

Table 3–11 shows the section and channel assignments for the Async group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–11: Async group channel assignments

Bit order	Section:channel	80186/80188 signal name
4	C0:4	SRDY*
3	C0:3	ARDY*
2	C0:2	RD~*
1	C0:1	WR~*
0	C0:0	ALE~*

*** Signal not required for disassembly.**

Table 3–12 shows the section and channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects.

Table 3–12: Clock group channel assignments

Bit order	Section:channel	80186/80188 signal name
CLK:3	CLK	CLKOUT
CLK:2	QUAL	STATUS
C2:1	QUAL	HLDA
C2:0	QUAL	RESET

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–12, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires 80186/80188 signals using the TMS 102 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 80186 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 80186/80188 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

Figure 3–3 shows the sample points and the master sample point.

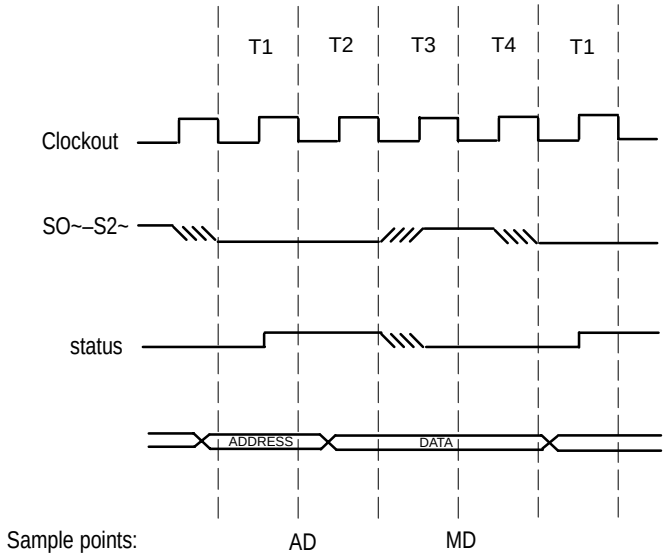


Figure 3–3: 80186/80188 Clocking

DMA Cycles

DMA cycles may be observed only as seen by the 80186/80188 microprocessor. System buffering of the address, data, and control lines must be organized so they point to the 80186/80188 microprocessor, and enabled so the DMA cycles are visible to the probe adapter at the 80186/80188 socket. You may need to modify the SUT to meet these requirements if you want to monitor DMA cycles.

When DMA cycles are included, the HLDA signal is given special attention, and DMA cycles are distinguished from other ordinary 80186/80188 cycles. DMA cycles are included along with other 80186/80188-initiated cycles if the 80186/80188 bus transfer protocol is followed, and if the SUT bus buffering topology provides adequate data visibility at the 80186/80188 socket. If these conditions are not met, a special sample is forced to record a transfer of bus mastership.

The 80186/80188 use a 20R6–5ns PAL on the probe adapter to decode the status lines (S0~, S1~, and S2~) and generate a signal called STATUS, which is used to determine the sample points for the disassembler. The status lines become valid after the rising edge of CLKOUT, indicating the start of a bus cycle. At the next rising edge of CLKOUT, the status signal is asserted. The status lines and STATUS signal become invalid several clock cycles later after the falling edge of CLKOUT, indicating the end of a bus cycle.

Clocking Options

The clocking algorithm for the 80186/80188 support has two variations: DMA Cycles Excluded and DMA Cycles Included.

DMA Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles initiated by the 80186/80188 microprocessor (HLDA low) will be logged in. Backoff cycles (caused by the BOFF# signal) are stored.

DMA Cycles Included. All bus cycles, including Alternate Bus Master cycles and Backoff cycles, are logged in.

When the HLDA signal is high, the microprocessor has given up the bus to an alternate device. The design of the 80186/80188 system affects what data will be logged in. The module only samples the data at the pins of the microprocessor. To properly log in bus activity, any buffers between the microprocessor and the alternate bus master must be enabled and pointing at the microprocessor.

There are three possible 80186/80188 system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

- If the alternate bus master drives the same control lines as the 80186/80188 microprocessor, and the microprocessor “sees” these signals, the bus activity is logged in like for normal bus cycles except that the HLDA signal is high.
- If none of the control lines are driven or if the 80186/80188 microprocessor can not see them, the module will still clock in an alternate bus master cycle. The information on the bus at one clock prior to the HLDA signal going low is logged in. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the address that gets logged in will be the “next address,” not the address that occurred one clock before the HLDA signal went low.
- If some of the 80186/80188 microprocessor control lines are visible (but not all), the module logs in what it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HLDA signal going low. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the “next address” will be logged in instead of the previously saved address.

When the BOFF# signal goes low (active), a backoff cycle has been requested and the 80186/80188 microprocessor gives up the bus on the next clock cycle. The module aborts the bus cycle that it is currently logging in (the 80186/80188 microprocessor will restart this cycle once the BOFF# signal goes high). A backoff cycle will be logged in using one of the three interactions described for the HLDA signal (except that the BOFF# signal is stored as a low-level signal in each of the cases).

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

All 80186/80188 microprocessor signals are accessible on the probe adapter.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The 80186/80188 use a 20R6–5 ns PAL on the probe adapter to decode the status lines (S0~, S1~, and S2~) and generate a signal called STATUS, which is used to determine the sample points for the disassembler. The status lines become valid after the rising edge of CLKOUT, indicating the start of a bus cycle. At the next rising edge of CLKOUT, the status signal is asserted. The status lines and STATUS signal become invalid several clock cycles later after the falling edge of CLKOUT, indicating the end of a bus cycle.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 102 80186/80188 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

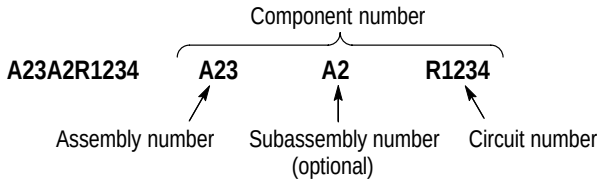
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
22526	BERG ELECTRONICS INC (DUPONT)	857 OLD TRAIL RD	ETTERS PA 17319
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671–2433–00			CIRCUIT BD ASSY:80186/188,PGA68 SOCKETED PROBE ADAPTER;	80009	671243300
A02	671–2577–00			CIRCUIT BD ASSY:80186/188,PROBE ADAPTER, SUB	80009	671257700
A01	671–2433–00			CIRCUIT BD ASSY:80186/188,PGA68 SOCKETED PROBE ADAPTER;	80009	671243300
A01C210	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01C230	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01C315	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,SMD,T&R	TK0875	267M–1002–476–K
A01C320	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01J120	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J300	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J340	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J520	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235		
A01U220	160–8860–00			IC,DIGITAL:STTL,PLD;PAL,20R6,5NS,210MA,STATUS MONITOR	80009	160–8860–00
A01U320	—— ——			SOCKET,PGA:PCB,;68 POS,11 X 11,0.1 CTR X 0. 1 CTR 0.17 H X 0.273 TAIL,OPEN CTR, SYMMETRICAL,PAT 1189 (SEE RMPL)		
A02	671–2577–00			CIRCUIT BD ASSY:80186/188,PROBE ADAPTER, SUB	80009	671257700
A02C210	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A02C230	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A02C240	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,SMD,T&R	TK0875	267M–1002–476–K
A02C540	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A02J120	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)	80009	131526700
A02J300	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)	80009	131526700
A02J340	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)	80009	131526700
A02J520	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)	80009	131526700
A02P320	—— ——			CONN,ADPT:SMD,PLCC;MALE,STR,68 POS,0.05 CTR,0.268H, PLCC MALE TOSMD PADS (SEE RMPL)		
A02U220	160–8860–00			IC,DIGITAL:STTL,PLD;PAL,20R6,5NS,210MA, STATUS MONITOR	80009	160–8860–00
A02U320	—— ——			SOCKET,PLCC:SMD,;68 POS,0.05 CTR,0.200 H,TIN, ACCOM 0.055–0.095 (SEE RMPL)		

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 102 80186/80188 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2358	EMULATION TECHNOLOGY INC	2368B WALSH AVE, BLDG D	SANTA CLARA CA 95051
05276	ITT POMONA ELECTRONICS DIV	1500 E 9TH ST PO BOX 2767	POMONA CA 91766–3835
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0543–00			1	PROBE ADAPTER:80186/188,PGA68 SOCKETED;	80009	010054300
–1	136–1023–00			1	SKT,PL–IN ELEK:MICROCKT,68 CONTACT,LCC (USED WITH 136–0921–00 TO FORM LCC–TO PGA TESTCLIP)	53387	2–0068–05400–08
–2	136–0921–00			1	SOCKET,PGA::PCB,;68 POS,11 X 11,0.1 CTR,0.170 H X 0.183 TAIL,OPEN CTR,SYMMETRICAL (USED WITH 136–1023–00 TO FORM A LCC TO PGA TESTCLIP)	63058	PGA 68H101B1–11
–3	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J120,J300,J340,J520)	80009	131526700
–4	671–2433–00			1	CIRCUIT BD ASSY:80186/188,PGA68 SOCKETED PROBE ADAPTER;	80009	671243300
–5	136–0922–00			2	SOCKET,PGA:PCB,;68 POS,11 X 11,0.1 CTR X 0.1 CTR 0.17 H X 0.273 TAIL,OPEN CTR, SYMMETRICAL, PAT 118 (U320)	63058	PGA 68H115B1–11
					STANDARD ACCESSORIES		
	070–8866–00			1	MANUAL,TECH:92DM06A,INSTRUCTION,80186/8,DISASSEMBLER	80009	070886600
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
–6	103–0294–00			1	ADAPTER,CONN:80186/80188 68 PIN LCC TO 68 PIN PGA	TK2358	AP3–68–PGA–G
–7	013–0250–00			1	ADAPTER,TEST:68 PIN PLCC (USED WITH 103–0311–00 TO FORM A LCC–TO PGA TESTCLIP)	05276	E11886
–8	103–0311–00			2	ADAPTER,CONN:80186/188 68 PIN PGA TO PLCCQUAD TEST CLIP (U230) (USED WITH 013–0250–00 TO FORM A LCC–TO PGA TESTCLIP)	TK2358	AC–PGA–PCC–808

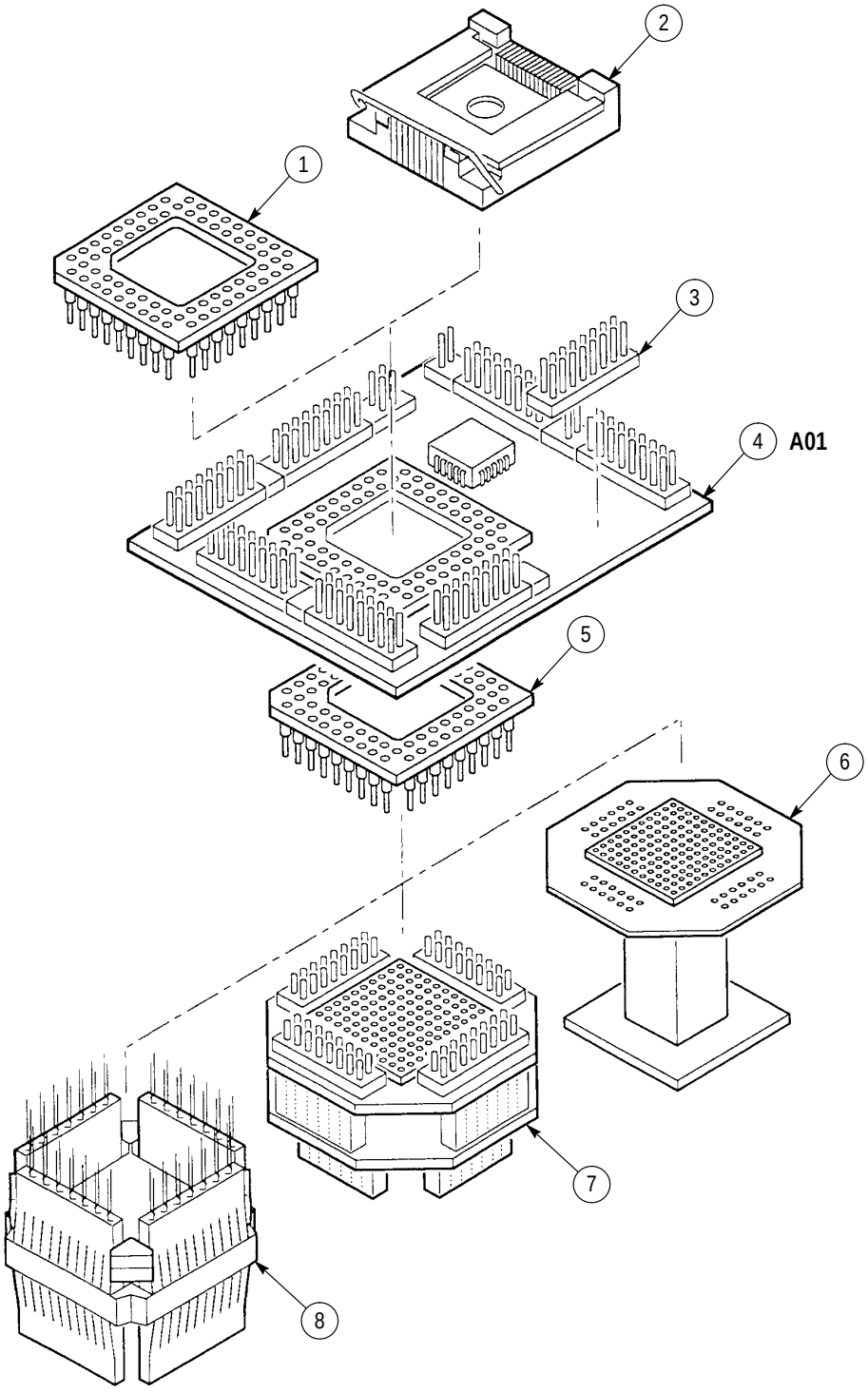


Figure 6–1: 80186/80188 PGA probe adapter exploded view

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2-1	671–2577–00			1	CIRCUIT BD ASSY:80186/188,PROBE ADAPTER, SUB PLCC68, SOCKETED,;	80009	671257700
–2	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J120,J300,J340,J520)	80009	131526700
					STANDARD ACCESSORIES		
	070–8866–00			1	MANUAL,TECH:92DM06A,INSTRUCTION, 80186/8,DISASSEMBLER	80009	070886600

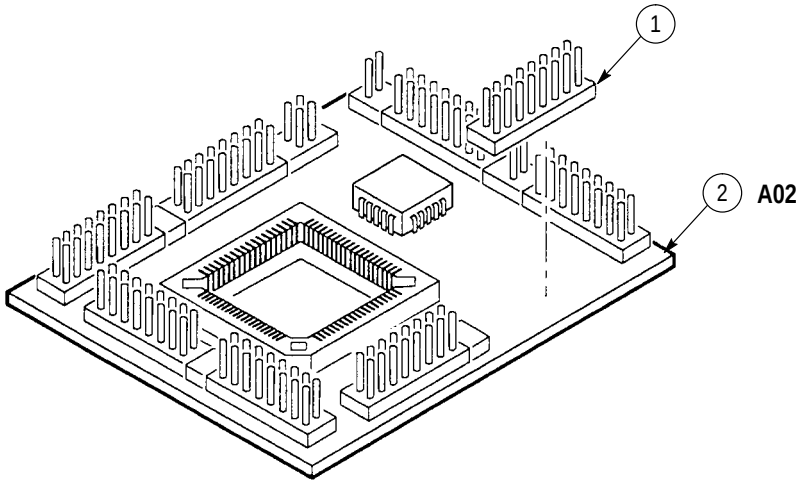


Figure 6–2: 80186/80188 PLCC probe adapter exploded view

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DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. Logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.15, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

Electrical components shown on the diagram are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads(pF)
Values less then one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICATORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (/) following the signal name (e.g., RESET~ or RESET/).

The information and special symbols below may appear in this manual.

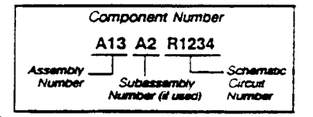
ASSEMBLY NUMBERS

Each assembly in the instrument is assigned an assembly number (e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location illustration
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

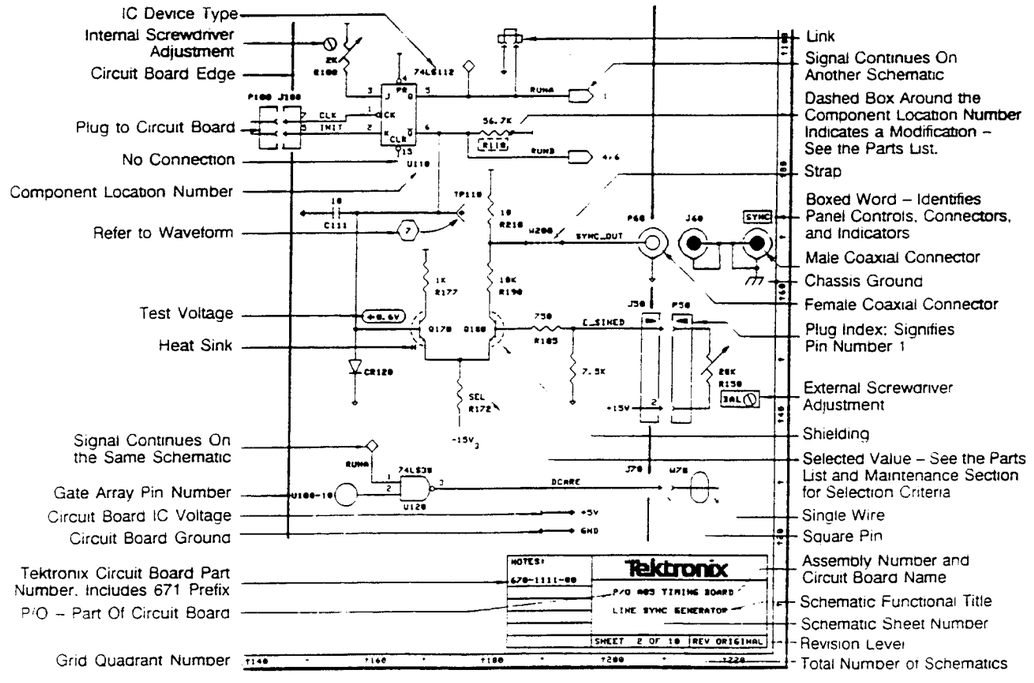
COMPONENT NUMBER EXAMPLE

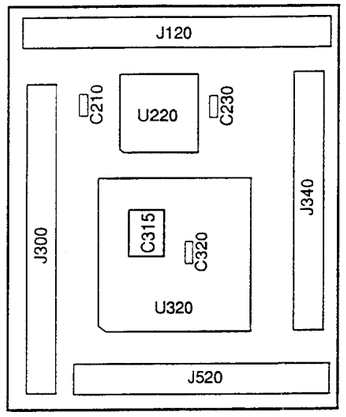


Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

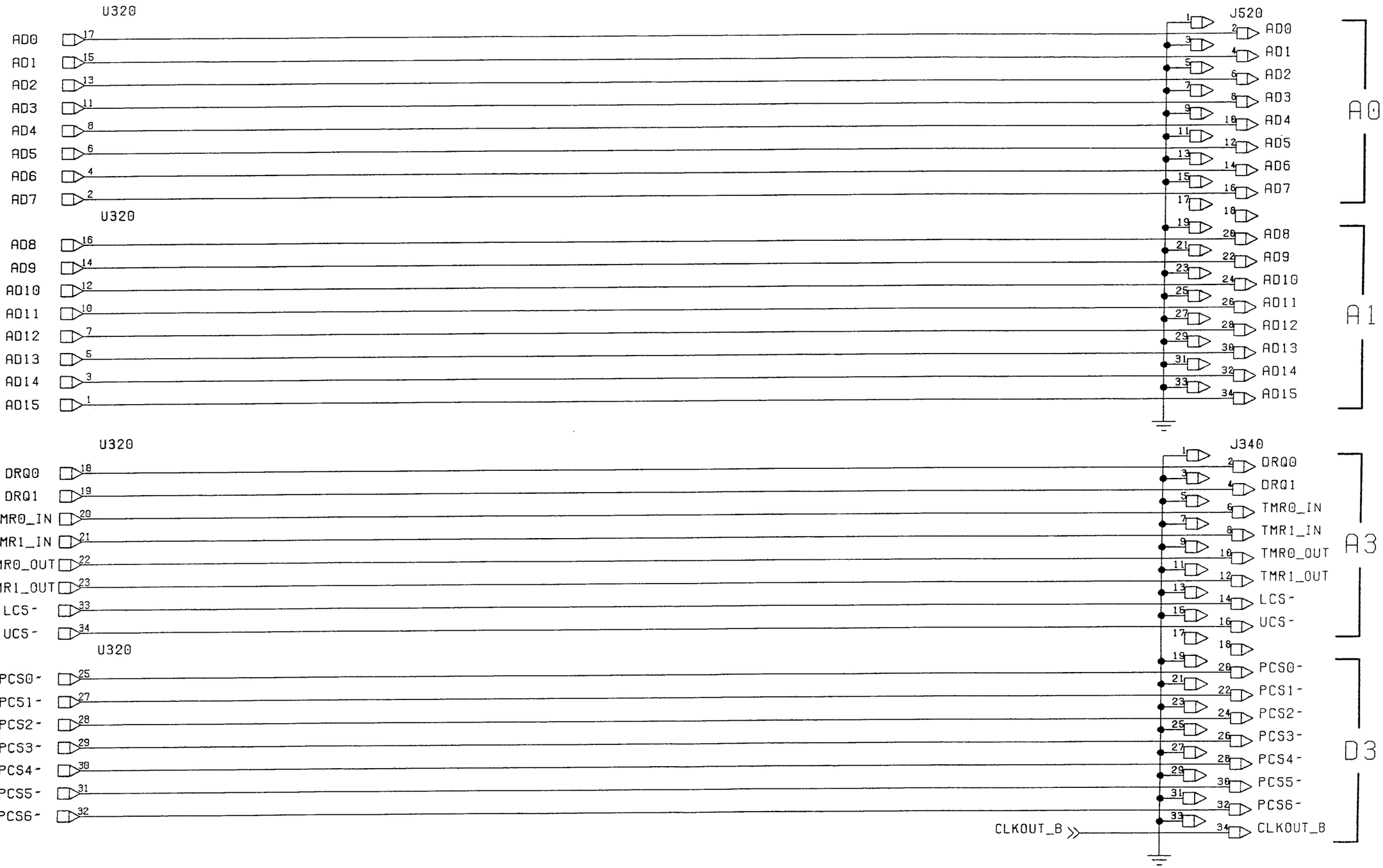
GRID COORDINATES

The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).





A01 80186/80188 PGA probe adapter board component locations



TEKTRONIX	A01	80186/188 Microprocessor Probe Adapter LASI III	DATE: 8-26-91
671-2433-00			SHEET 1 OF 3

U320

MCS0- 38
MCS1- 37
MCS2- 36
MCS3- 35
INT0 45
INT1 44
INT2 42
INT3 41

U320

RESET 57
HLDA 51
S0- 52
S1- 53
S2- 54
LOCK- 48
NMI 46
TEST- 47

CLKOUT 56

20R6_SPLC
160-8860-00

U220

CLKOUT_B

U320

ALE 61
WR- 63
RD- 62
ARDY 55
SRDY 49

RES- 24

J120

1 2 MCS0-
3 4 MCS1-
5 6 MCS2-
7 8 MCS3-
9 10 INT0
11 12 INT1
13 14 INT2
15 16 INT3
17 18
19 20 CLKOUT
21 22
23 24 RESET
25 26 HLDA
27 28 S0-
29 30 S1-
31 32 S2-
33 34 LOCK-
35 36 NMI
37 38 TEST-
39 40
41 42 STATUS

C3

CK3

C2

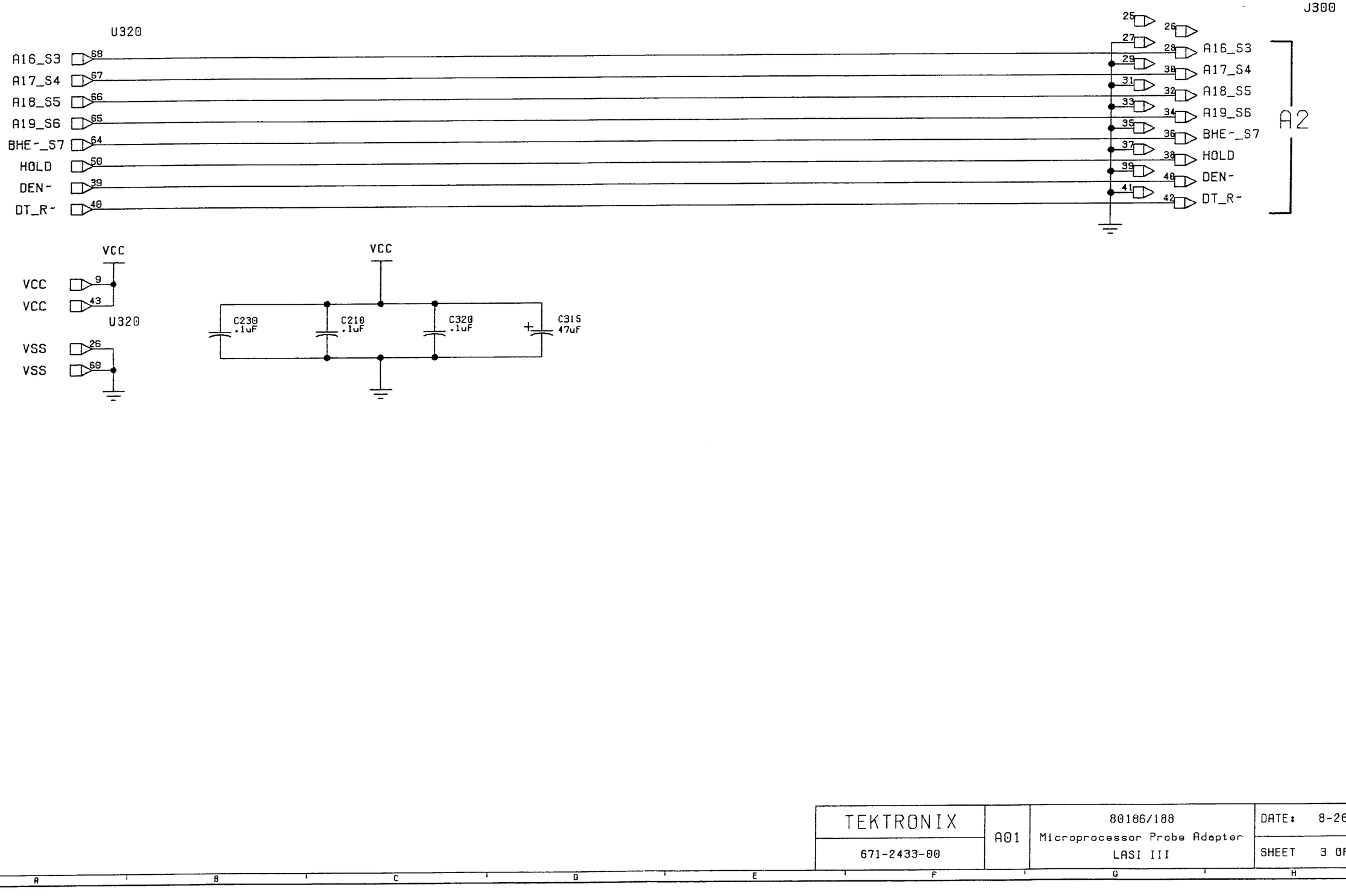
CK2

J300

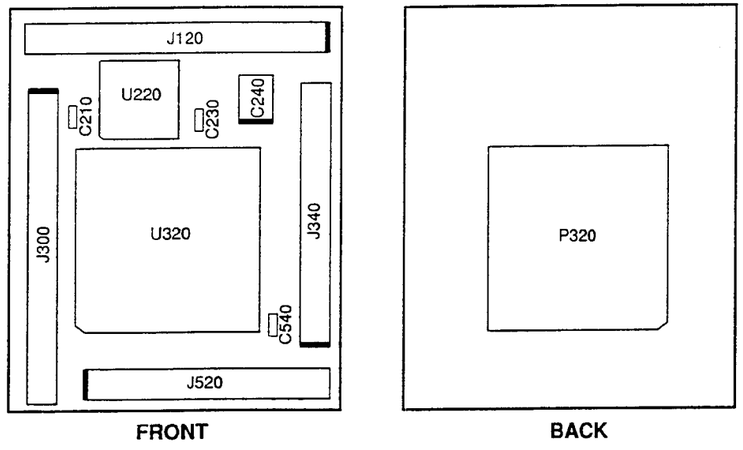
1 2 RES-
3 4 NMI
5 6
7 8
9 10 ALE
11 12 WR-
13 14 RD-
15 16 ARDY
17 18 SRDY
19 20
21 22
23 24

AUX/C0

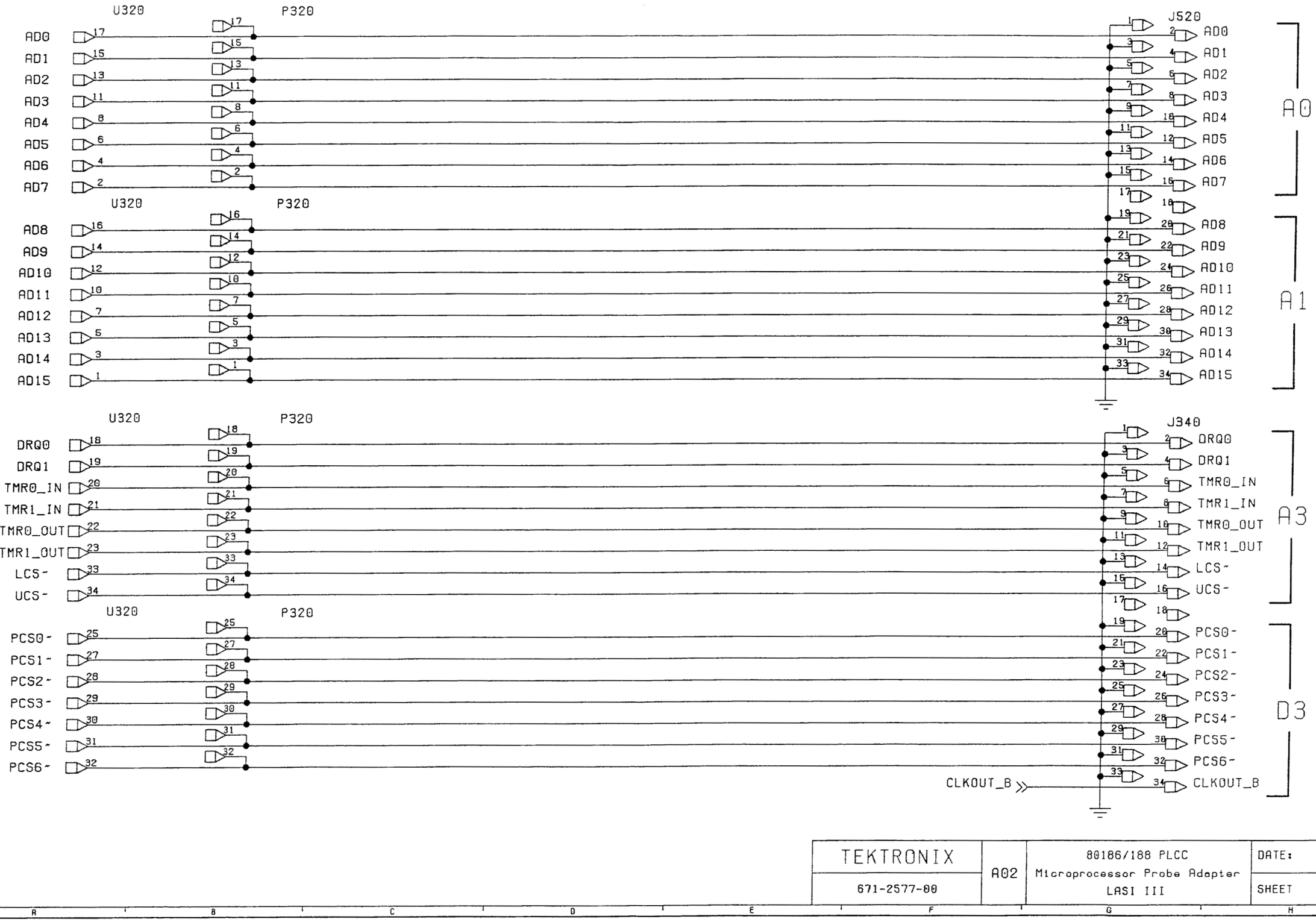
TEKTRONIX	A01	80186/188 Microprocessor Probe Adapter LASI III	DATE: 8-26-91
671-2433-00			SHEET 2 OF 3



TEKTRONIX	A01	80186/188 Microprocessor Probe Adapter LASI III	DATE: 8-26-91
671-2433-00			SHEET 3 OF 3



A02 80186/80188 PLCC probe adapter board component locations



TEKTRONIX	A02	80186/188 PLCC Microprocessor Probe Adapter LASI III	DATE: 8-26-91
671-2577-00			SHEET 1 OF 3

U320 P320

MCS0- 38 → 38
MCS1- 37 → 37
MCS2- 36 → 36
MCS3- 35 → 35
INT0 45 → 45
INT1 44 → 44
INT2 42 → 42
INT3 41 → 41

U320 P320

RESET 57 → 57
HLDA 51 → 51
S0- 52 → 52
S1- 53 → 53
S2- 54 → 54
LOCK- 48 → 48
NMI 46 → 46
TEST- 47 → 47

CLKOUT 56 → 56

20R6_SPLC
160-8860-00

U220

2, 16, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 17, 27 → 26, 25, 24, 23, 21, 20, 19, 18

CLKOUT_B

U320 P320

ALE 61 → 61
WR- 63 → 63
RD- 62 → 62
ARDY 55 → 55
SRDY 49 → 49

RES- 24 → 24

J120

1	2	MCS0-
3	4	MCS1-
5	6	MCS2-
7	8	MCS3-
9	10	INT0
11	12	INT1
13	14	INT2
15	16	INT3
17	18	
19	20	CLKOUT
21	22	
23	24	RESET
25	26	HLDA
27	28	S0-
29	30	S1-
31	32	S2-
33	34	LOCK-
35	36	NMI
37	38	TEST-
39	40	
41	42	STATUS

C3

CK3

C2

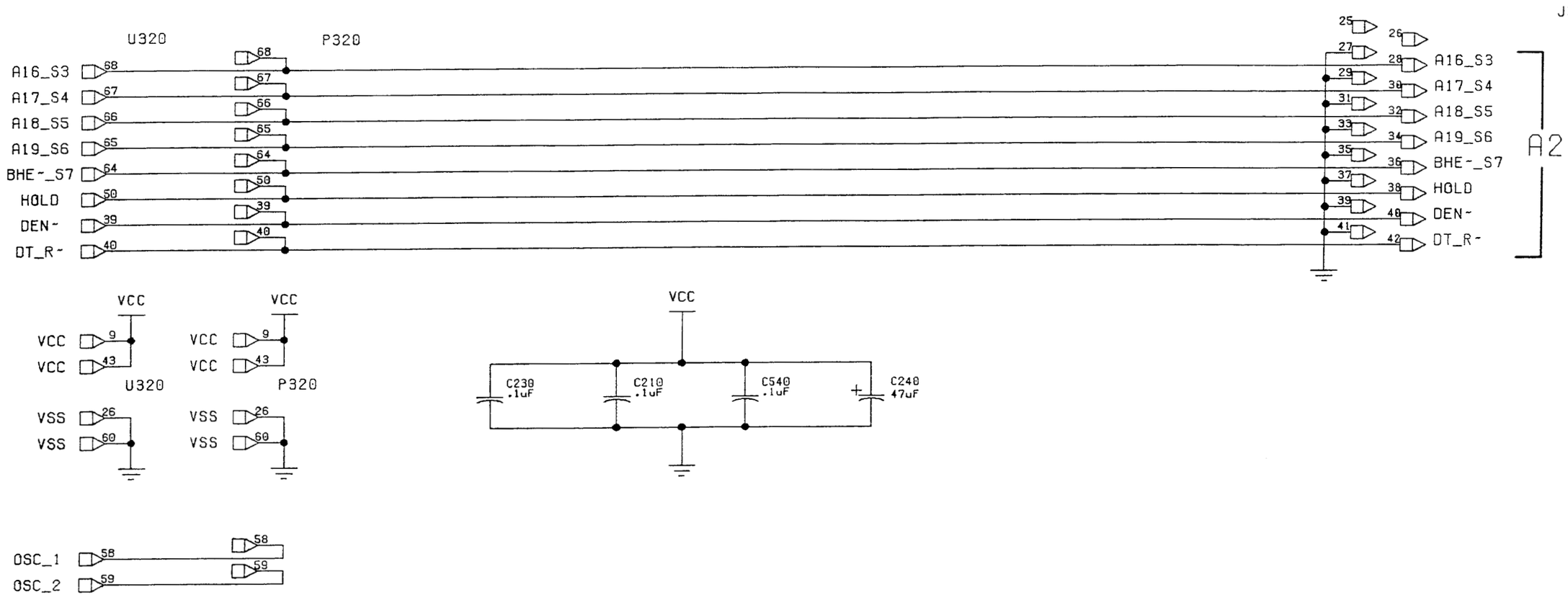
CK2

J300

1	2	RES-
3	4	NMI
5	6	
7	8	
9	10	ALE
11	12	WR-
13	14	RD-
15	16	ARDY
17	18	SRDY
19	20	
21	22	
23	24	

AUX/C0

TEKTRONIX	A02	80186/188 PLCC Microprocessor Probe Adapter LASI III	DATE: 8-26-91
671-2577-00			SHEET 2 OF 3



TEKTRONIX	A02	80186/188 PLCC Microprocessor Probe Adapter LASI III	DATE: 8-26-91
671-2577-00			SHEET 3 OF 3